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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/890,471 | 08/01/2001 | N. Edward Berg | BERG99.01CIP | 3251 |

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HAYES, SOLOWAY P.C.
130 W. CUSHING STREET
TUCSON, AZ 85701

| EXAMINER | |
|---|---|
| CULBERT, ROBERTS P | |
| **ART UNIT** | **PAPER NUMBER** |
| 1763 | |

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/890,471 | BERG, N. EDWARD | |
| | Examiner | Art Unit | |
| | Roberts Culbert | 1763 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *41-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 41-59 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification of the present application teaches a method of forming a circuit board comprising: forming first and second conductor layers on a non-conducting substrate (Fig 1. and Page 4, Line 31 – Page 5, Line 11), pre-heating the substrate and forming first and second pattern masks on the conductor layers to leave exposed portions of the conductor layers (Fig 2. and Page 5, Lines 12-29), plating the exposed portions of the conductor layers (Fig 3. and Page 5, Lines 30-31) and removing the pattern masks and underlying conductor layers (Fig 4. and Page 5, Line 31 – Page 6, Line 3). Next, vias are drilled and plated in the substrate. (Figures 5-11) and circuit elements are printed on the circuit board by printing a resist and plating or by printing conductive ink. (Fig. 12-21) Finally multiple layer boards may be formed by lamination. (Fig 22-24)

Regarding Claims 41 and 48, applicant does not provide an embodiment of the invention in which a circuit board substrate is preheated prior to forming an etch resist mask or prior to an etching step. Applicant discloses the preheating step only prior to forming a plating mask and subsequent plating step. Therefore there is no support in the original written disclosure for preheating a substrate, forming a resist mask on the substrate to form exposed areas and then etching the exposed areas to form void areas as recited in claims 41 and 48. Although etching is performed after the plating step to remove a portion of the conductor layer, the etching is not performed on the exposed areas of the conductor, (not covered by the mask) but on the unexposed regions (areas that are covered by the mask).

Claims 46 and 47, recite that the step of printing a conductive composition further comprises printing a resist mask, plating etc. However, applicant does not provide an embodiment of the invention in which a conductive composition is printed in combination with the steps of printing a resist mask and plating. The present invention only teaches the resist mask and plating steps are an alternative technique to the step of printing patterns with a conductive composition (ink).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 41, 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,359,516 to Nacci et al. in view of U.S. Patent 4,501,638 to Johnson and in further view of U.S. Patent 5,132,248 to Drummond et al.**

Nacci et al. teaches a method of manufacturing a circuit board comprising providing a non-conducting substrate having a top surface and a bottom surface, the top surface comprising a first conductor and the bottom surface comprising a second conductor (Col. 10, Line 67 – Col. 11, Line 41); preheating the substrate (Col. 3, Lines 10-14) and image printing a resist mask over a portion of the first conductor to form a plurality of first exposed areas; image printing a resist mask over a portion of the second conductor to form a plurality of second exposed areas, wherein each of the plurality of first exposed areas is disposed above one of the plurality of second exposed areas;

Nacci et al. does not teach the step of forming vias in the circuit board. However, the step of forming through-holes or vias through a multi-sided circuit board substrate is notoriously old and well known in the circuit board manufacturing art.

Johnson teaches one of several known methods of forming conductive vias in a circuit board substrate. Johnson teaches removing a first conductor from each of the plurality of first exposed areas to

form a plurality of first void areas on the top surface (Fig 2A); removing the second conductor from each of the plurality of second exposed areas to form a plurality of second void areas on the bottom surface (Fig 2A); forming a plurality of vias by connecting one of the plurality of first void areas with one of the plurality of second void areas (Fig 2B); plating the plurality of vias to form the plurality of conductive pathways between the top surface and the bottom surface; (Col. 3, Lines 60-65)

It would have been obvious to one of ordinary skill in the art at the time of invention to form conductive vias as shown in Johnson through the circuit board substrate of Nacci et al.

One of ordinary skill in the art would have been motivated at the time of invention to perform the conventional step in order to provide electrical interconnection between circuit elements on the front and back sides of the circuit board.

Nacci et al. in view of Johnson does not teach printing a conductive composition onto the circuit board substrate.

Drummond et al. teaches a method of forming the conductive circuit patterns on a circuit substrate. Drummond et al teaches forming a circuit pattern on the circuit substrate surface by direct image printing a conductive ink composition onto the top surface using an inkjet printing technique.

It would have been obvious to one of ordinary skill in the art at the time of invention to use the circuit forming technique of Drummond et al. to form circuit patterns on the circuit board substrate of Nacci et al. in view of Johnson.

One of ordinary skill in the art would have been motivated at the time of invention to use the circuit forming technique of Drummond et al. in order to provide a multisided circuit board having circuit patterns that are interconnected by the plated through holes or vias.

Regarding Claims 46 and 47 Nacci et al. teaches that the circuit board patterns may be formed by direct image printing a resist mask, plating the top surface to increase thickness, removing the mask, and removing exposed conductor (Col. 10, Lines 34-55)

**Claims 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,359,516 to Nacci et al. in view of U.S. Patent 4,501,638 to Johnson and U.S. Patent 5,132,248 to Drummond et al. and in further view of UK Patent GB 2227887 A to Lowe et al.**

Regarding Claims 42-45, Nacci et al. in view of Johnson and Drummond et al. teach the method of the invention substantially as claimed, but do not teach the step of printing circuit devices such as resistors and capacitors and solder-resist masks on the circuit board substrate.

Lowe teaches that the conductive layers, circuit devices and solder-resist masks of a circuit board may be formed by etching or by direct printing using screen-printing, transfer printing, lithographic printing or other methods. See Abstract, Examples and (Page 8, Lines 7-9), (Page 10, Lines 10-20) and (Page 18). It would have been obvious to one of ordinary skill in the art at the time of invention to use a printing technique such as lithography to form the conductive layers, circuit devices and resist masks of a circuit board since Lowe teaches that the techniques are equivalent methods of forming the conductive patterns, circuit devices and resist masks. Note also that since Lowe teaches that any printing method is acceptable that will handle the conducting, resistive, carbon and solder resist inks.

**Claims 48 and 51-59 are is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,359,516 to Nacci et al. in view of U.S. Patent 4,501,638 to Johnson and U.S. Patent 5,132,248 to Drummond et al. and in further view of U.S. Patent 4,526,835 to Takahashi et al.**

Regarding Claim 48, Nacci et al. in view of Johnson and Drummond et al. teach the method of the invention substantially as claimed, but do not teach the steps of joining two circuit board substrates using an insulating layer and forming conductive pathways between the circuit patterns.

Takahashi et al. teaches a method of forming a multilayer circuit board comprising laminating a plurality of circuit board substrates together using an insulating layer. Next, plated through holes or vias are formed connecting the circuit patterns the circuit board substrates. (See Figures 1 - 4B and the related discussion)

It would have been obvious to one of ordinary skill in the art at the time of invention to join multiple circuit board substrates using an insulating layer and then interconnecting the circuit patterns using plated through holes as shown in Takahashi et al.

One of ordinary skill in the art would have been motivated at the time of invention to join multiple circuit boards in order to form a completed multilayer circuit board as shown by Takahashi et al.

Regarding Claims 51, 52, 54, 55, 58 and 59 Nacci et al. teaches that the circuit board patterns may be formed by direct image printing a resist mask, plating the top surface to increase thickness, removing the mask, and removing exposed conductor (Col. 10, Lines 34-55)

**Claims 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,359,516 to Nacci et al. in view of U.S. Patent 4,501,638 to Johnson, U.S. Patent 5,132,248 to Drummond et al. and U.S. Patent 4,526,835 to Takahashi et al. and in further view of UK Patent GB 2227887 A to Lowe et al.**

Regarding Claims 49 and 50, Nacci et al. in view of Johnson and Drummond et al. teach the method of the invention substantially as claimed, but do not teach the step of printing circuit devices such as resistors and capacitors on the circuit board substrate.

Lowe teaches that the conductive layers, circuit devices and solder-resist masks of a circuit board may be formed by etching or by direct printing using screen-printing, transfer printing, lithographic printing or other methods. See Abstract, Examples and (Page 8, Lines 7-9), (Page 10, Lines 10-20) and (Page 18). It would have been obvious to one of ordinary skill in the art at the time of invention to use a printing technique such as lithography to form the conductive layers, circuit devices and resist masks of a circuit board since Lowe teaches that the techniques are equivalent methods of forming the conductive patterns, circuit devices and resist masks. Note also that since Lowe teaches that any printing method is acceptable that will handle the conducting, resistive, carbon and solder resist inks.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberts Culbert whose telephone number is (571) 272-1433. The examiner can normally be reached on Monday-Friday (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

R. Culbert

R. Culbert

PARVIZ HASSANZADEH
SUPERVISORY PATENT EXAMINER